# IEEE Oregon Joint EPS/CASS Chapter Seminar

**6.00–7.30pm PT Thursday, January 21st, 2021**

**Virtual Online**

**All Welcome**

**Free Registration Required:**
**https://meetings.vtools.ieee.org/event/register/252737**

**(A WebEx link will be sent to all registrants one day beforehand.)**

# "Flexible Hybrid Electronics 2.0"

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## Abstract

In the last few years, electronics packaging has rightfully emerged from the shadows of CMOS scaling to make a significant impact in high performance and mobile appliance computing. The area of Flexible Hybrid Electronics (FHE) has also developed and is making a significant impact in the area of medical and wellness electronics. The first generation of these devices have, for most part, adapted Printed Circuit Board (PCB) technology by using thinner PCBs and assembling either thinned or thin packaged "older" generation of chips on to these platforms, typically with coarse printed wiring to connect a small number of such chips. This approach, while immensely useful to get the field going, needs to adapt and borrow from the both silicon and advanced packaging technology trends, so that we can advance this trend to the next level. The key paradigm challenges ahead are: scaling the FHE in general – this includes the adoption of dielet (chiplet) technology in more advanced CMOS nodes including edge-AI, higher performance interconnects, flexible high-density energy storage, wireless communication and advanced ergonomics and all of these at lower cost and higher reliability. In this talk we will address these challenges and outline a possible technology roadmap to achieve these goals in the next few years.

## Speaker Biography

**Subramanian S. Iyer** (Subu) is Distinguished Professor and holds the Charles P. Reames Endowed Chair in the Electrical Engineering Department and a joint appointment in the Materials Science and Engineering Department at the University of California at Los Angeles. He is Director of the Center for Heterogeneous Integration and Performance Scaling (CHIPS). Prior to that he was an IBM Fellow. His key technical contributions have been the development of the world's first SiGe base HBT, Salicide, electrical fuses, embedded DRAM and 45nm technology node used to make

the first generation of truly low power portable devices as well as the first commercial interposer and 3D integrated products. He also was among the first to commercialize bonded SOI for CMOS applications through a start-up called SiBond LLC. More recently, he has been exploring new packaging paradigms and device innovations that they may enable wafer-scale architectures, in-memory analog compute and medical engineering applications. He has published over 300 papers and holds over 75 patents. He has received several outstanding technical achievements and corporate awards at IBM. He is an IEEE Fellow, an APS Fellow and a Distinguished Lecturer of the IEEE EDS and EPS and a member of the Board of Governors of IEEE EPS. He is also a Fellow of the National Academy of Inventors and iMAPS. He is a Distinguished Alumnus of IIT Bombay and received the IEEE Daniel Noble Medal for emerging technologies in 2012 and the 2020 iMAPS Daniel C. Hughes Jr Memorial award.

List of publications/patents:
https://scholar.google.com/citations?user=xXV4oIMAAAAJ&hl=en